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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,450	12/02/2004	Chen-Chih Huang	SUND 501CIP	3611

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,450	HUANG ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/079,866.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to Applicant's amendment filed on 02/14/2007. By virtue of this amendment, claims 17-21 are newly added; thus, claims 1-21 are currently presented in the instant application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-9, 12-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1A) in view of Tomobe et al. (U.S. Patent No. 6,198,334).

With respect to claims 1, 4-7, 9, 12-15, 17 and 20-21, the Applicant's Admitted Prior Art (Fig. 1A) discloses a phase-interpolation circuit for outputting a third clock signal, the circuit comprising (1) a first inverter [11] for receiving a first clock signal [CK1], and (2) a second inverter [12] for receiving a second clock signal [CK2], and an output end connected to an output end of the first inverter to form a common output end [V0] to output the third clock signal; in which the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal.

The Applicant's Admitted Prior Art (Fig. 1) does not disclose a detailed configuration of the inverters, including (1) a first controlled switch connecting between the first inverter, the second inverter, and a power source; wherein the first controlled switch is (i) "OFF" when the

first clock signal is in a first state *(or when both the first and second double-level clock signals are in the first state)*, and (ii) is "ON" when the first clock signal is in a second state *(or when both the first and second clock signals are in the second state)*, (2) a second controlled switch connecting between the first inverter, the second inverter, and ground; in which (i) the second controlled switch is "ON" when the first clock signal is in the first state *(or when both the first and second clock signals are in the first state)*, and (ii) is "OFF" when the first clock signal is in the second state *(or when both the first and second clock signals are in the second state)*, (3) (including limitations claimed in claim 4) a first PMOS connecting between the first inverter and the power source, being "OFF" when the first clock signal is in the first state, and being "ON" when the first clock signal is in the second state; a second PMOS connecting between the second inverter and the power source, being "OFF" when the second clock signal is in the first state *(or when both the first and second clock signals are in first state)*, and being "ON" when the second clock signal is in the second state *(or when both the first and second clock signals are in second state)*, and the first controlled switch and the second controlled switch are to avoid a short circuit current of the phase-interpolation circuit (4) (including limitations claimed in claim 5) a first NMOS connecting between the first inverter and the ground, being "OFF" when the first clock signal is in the second state *(or when both the first and second clock signals are in the second state)*, and being "ON" when the first clock signal is in the first state *(or when both the first and second clock signals are in the first state)*; a second NMOS connecting between the second inverter and the ground, being "OFF" when the second clock signal is in the second state *(or when both the first and second clock signals are in the second state)*, and being "ON" when the first clock signal is in the first state *(or when both the first and second clock signals are in the*

first state), (5) (including limitations claimed in claim 6) the first controlled switch being (i) a PMOS, and (6) (including limitations claimed in claim 7) the second controlled switch being (i) an NMOS.

Tomobe et al. discloses, in Fig. 1, a detailed configuration of a CMOS inverter circuit. The CMOS inverter circuit comprises (1) an input end [INPUT TERMINAL], (2) a first controlled switch [P1], (3) a CMOS inverter [P2, N2], and (4) a second controlled switch [N1]; wherein all [P1, P2, N1, N2] are connected in series.

To modify the phase interpolation circuit of the Applicant's Admitted Prior Art (Fig. 1A) by configuring in the CMOS inverters of the Applicant's Admitted Prior Art (Fig. 1A) with the PMOS and NMOS transistors connected in series in each inverter to cause switching speeds of the transistors and thus to improve the noise resistance performance of the phase interpolation circuit would have been obvious to one of ordinary skills in the art at the time of the invention since such a configuration of the PMOS and NMOS transistors in the CMOS inverters for the stated purpose has been a well-known practice in the art as evidenced by the teachings of Tomobe et al. (see Tomobe et al.; Abstract, lines 1-7).

With respect to claims 8 and 16, the Applicant's Admitted Prior Art (Fig. 1A) teaches that the inverters are CMOS inverters (see page 4, line 6, of the specification of the instant application).

3. Claims 2-3, 10-11 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1A) in view of Tomobe et al. (U.S. Patent No.

6,198,334) as applied to claims 1, 9 and 17 above, and further in view of Kim (U.S. Patent No. 6,225,847).

With respect to claims 2, 10 and 18, the combined teachings of the Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. disclose all of the claimed limitations as expressly recited in claims 1, 9 and 17 above, except for a third inverter having (i) an input end connected to the common output end, and (ii) an output end for outputting a third clock signal.

Kim discloses, in Fig. 2, a CMOS clock generating circuit comprising an inverter [INV3] which has (i) an input end [34] connected to the common output end [output of element 3], and (ii) an output end for outputting a clock signal [Clk].

It would have been obvious to one of ordinary skill in the art at the time of the invention to additionally configure in the interpolation circuit of the combination The Applicant's admitted Prior art (Fig. 1A) and Tomobe et al. an inverter having an input end for connecting to the common output end (of the phase interpolation circuit of the combination) and an output end for outputting a clock signal as taught by Kim to obtain an inverted and buffered output clock signal since such an arrangement of the additional inverter would provide a complementary output clock signal that would be needed for a specific application to acquire an optimal performance.

With respect to claims 3, 11 and 19, the combined teachings of the Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. disclose all of the claimed limitations as expressly recited in claims 1 and 9 above, except for (1) an inverter (or a fourth inverter as claimed) having an output end connected to the first inverter in order to output the first double-level clock signal to the input end of the first inverter, and (2) another inverter (or a fifth inverter as claimed) having

an output end connected to the second inverter in order to output the second double-level clock signal to the input end of the second inverter.

Kim discloses, in figure 3, the configuration of an inverter [11] having (i) an input end [N1] connected to an input clock signal [Clk], and (ii) an output end [N2] for outputting an inverted clock signal [Clk\] to an input end [22] of an inverter [QP11, QN12]. Kim does not teach another inverter for a respective second inverter.

However, this practice of configuring an inverter for receiving an input clock signal and outputting an inverted clock signal to another inverter would provide complementary clock signals of exact phase and timing (see Kim, col. 2, lines 39-49), that would be needed for a specific application to acquire an optimal performance. For such an advantage, to implement the phase interpolation circuit of the combination The Applicant's Admitted Prior Art (Fig. 1A) and Tomobe et al. by arranging an inverter for receiving the input clock signal and outputting an inverted clock signal to a following inverter as taught by Kim would have been deemed obvious to a person skilled in the art.

Remark

4. Applicant's argument filed 02/14/2007 has been fully considered but they are not persuasive.

With respect to Applicant's argument regarding claims 1 and 9, at page 12, first paragraph, lines 5-6, that *the reference to Tomobe et al. illustrates inverter circuit with* ***only one input terminal for an input signal***; a) First, in response to Applicant's argument against the reference individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Clearly, it is the combination of all of the previously recited art (i.e. AAPA Fig. 1A and Tomobe et al.) that discloses a phase interpolation circuit with the claimed details, as can be seen in the previous office action rejection; b) Second, again it is the combination of AAPA Fig. 1A and Tomobe et al. that discloses the limitations of claims 1 and 9, Tomobe et al. discloses, in Fig. 1, an inverter with one input terminal for an input signal and AAPA Fig. 1A shows the structure of a phase interpolation circuit with two inverters. As such, the combined teachings of AAPA Fig. 1A and Tomobe et al.'s Fig. 1 disclose two inverters with two input terminals for two input signals amongst other claimed limitations, in claims 1 and 9.

Regarding Applicant's arguments still with respect to claims 1 and 9, at page 14, last paragraph, Applicant challenges the examiner's motivation for combining AAPA Fig. 1 and Tomobe et al.'s Fig. 1 to arrive at the claimed invention. First, motivation has been provided in the office action; and second, it is not necessary that the cited references or prior art actually suggest expressly or in so many words, the changes or improvements that the Applicant has made. The test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. In re Sheckier, 168 USPQ 716 (CCPA 1971) : In re McLaughlin 170 I USPQ 209 (CCPA 1971); In re Young 159 USPQ 725 (CCPA 1968).

In response to applicant's argument, at page 15, last paragraph, that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge

gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Similarly, at page 16, third paragraph, Applicant challenges the examiner's motivation for combining references. Response to this same argument has been provided in the paragraph above.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is 571-272-1749. The examiner can normally be reached on 7-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LMN

LINH MY NGUYEN
PRIMARY EXAMINER